

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type well and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and;

and

forming a silicide layer on a surface of the semiconductor substrate excluding the first

IN THE CLAIMS:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region;

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a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

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a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

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24. (Amended) A method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type well and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and; and

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